Exam

Power Electronics

Winter 2025/26

First name: Last name:

Matriculation number: Study program:

Instructions:

- You can only take part in the exam, if you are registered in the campus management system.
- Prepare your student ID and a photo ID card on your desk.
- Label each exam sheet with your name. Start a new exam sheet for each task.
- Answers must be given with a complete, comprehensible solution. Answers without any context will not be considered. Answers are accepted in German and English.
- Permitted tools are (exclusively): black / blue pens (indelible ink), triangle, a non-programmable calculator without graphic display and two DIN A4 cheat sheets.
- The exam time is 120 minutes.

Evaluation:

Task	1	2	3	4	$\sum$
Maximum score	8	10	13	11	42
Achieved score					

Task 1: Step-down converter **[8 Points]**

A drive system is powered by DC-voltage. The speed, position, and current sensors in the drive system require stable lower voltage. To transform the voltage down efficiently, a buck converter is used.

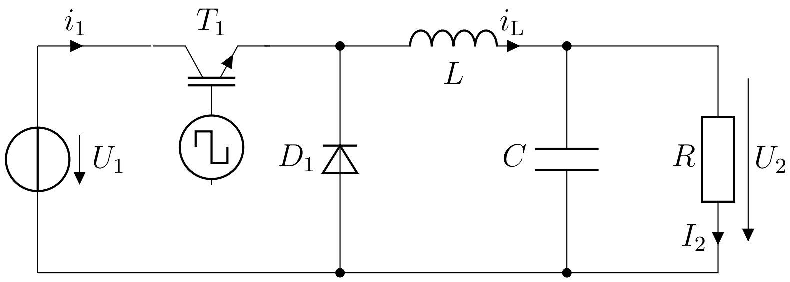


Fig. 1: Circuit with one transistor, filter and one load resistor.

General parameters:		**IGBT:**	
Input voltage:	$U_1 = 60$ V	Collector-emitter voltage:	$u_{\mathrm{on,CE}} = 2$ V
Output voltage:	$U_2 = 5.1$ V		
Output power:	$2.5\text{ W} \leq p \leq 15\text{ W}$	**Diode:**	
Switching frequency:	$f_\mathrm{s} = 100$ kHz	Forward voltage:	$u_{\mathrm{fw}} = 0.8$ V

Tab. 1: Parameters of the step-down converter.

1.1 What duty cycle must be set for the given input-to-output voltage ratio, assuming ideal components? [1 Point]

Answer:

The duty cycle corresponds to

$$D = \frac{U_2}{U_1} = \frac{60\text{ V}}{5.1\text{ V}} = 0.085.$$

1.2 What duty cycle is required when the voltage drops across the transistor and the diode are taken into account? [3 Points]

Answer:

In steady state, the inductor current balance is to apply:

$$\Delta i_{\mathrm{L,T_{on}}} \cdot T_{\mathrm{on}} = \Delta i_{\mathrm{L,T_{off}}} \cdot T_{\mathrm{off}}.$$

If the transistor conducts $\Delta i_{\mathrm{L,T_{on}}}$ results in:

$$\Delta i_{\mathrm{L,T_{on}}} = \frac{(U_1 - U_\mathrm{T} - U_2) \cdot T_{\mathrm{on}}}{L}.$$

If the transistor is blocking $\Delta i_{\mathrm{L,T_{off}}}$ is calculated by:

$$\Delta i_{\mathrm{L,T_{off}}} = \frac{(U_2 + u_{\mathrm{fw}}) \cdot T_{\mathrm{off}}}{L}.$$

By substituting the currents within the inductor current balance equation, we obtain

$$\frac{(U_1 - U_{\mathrm{T}} - U_2) \cdot T_{\mathrm{on}}}{L} = \frac{(U_2 + u_{\mathrm{fw}}) \cdot T_{\mathrm{off}}}{L}.$$

Replacing T_{on} and T_{off} by the switching period yields to

$$\frac{(U_1 - U_{\mathrm{T}} - U_2) \cdot T_{\mathrm{s}} \cdot D}{L} = \frac{(U_2 + u_{\mathrm{fw}}) \cdot (1 - D) \cdot T_{\mathrm{s}}}{L}.$$

After simplifying by canceling T_{s} and L, we obtain

$$(U_1 - U_{\mathrm{T}} - U_2) \cdot D = (U_2 + u_{\mathrm{fw}}) \cdot (1 - D).$$

Solving this equation with respect to D yields

$$D = \frac{U_2 + u_{\mathrm{fw}}}{U_1 - U_{\mathrm{T}} + u_{\mathrm{fw}}} = \frac{5.1\ \mathrm{V} + 0.8\ \mathrm{V}}{60\ \mathrm{V} - 2\ \mathrm{V} + 0.8\ \mathrm{V}} = 0.1.$$

1.3 The sensors have different power consumption depending on the operating point, i.e., $P_2 \in [2.5\ \mathrm{W}, 15\ \mathrm{W}]$ is given. Which load operating point is the relevant one to design the inductance value L such that discontinuous conduction mode (DCM) is always avoided? Calculate the minimal required inductances L for this case. [2 Points]

Answer:
The BCM mode occurs when the minimum average inductor current equals the half of the inductor current ripple. This leads to the operation point with minimal power consumption, which corresponds to the minimal current. The minimal average current $\bar{i}_1$ is expressed by

$$\bar{i}_{2,\mathrm{min}} = \frac{P_2}{U_2} = \frac{2.5\ \mathrm{W}}{5.1\ \mathrm{V}} = 0.49\ \mathrm{A}.$$

In case of boundary conduction mode following equation is to apply:

$$\Delta i_{\mathrm{L}} = 2 \cdot \bar{i}_{1,\mathrm{min}} = 2 \cdot 0.49\ \mathrm{A} = 0.98\ \mathrm{A}.$$

The ripple current Δi_{L} yields

$$\Delta i_{\mathrm{L}} = \frac{U_{\mathrm{L,on}} \cdot T_{\mathrm{on}}}{L} = \frac{(U_1 - U_{\mathrm{T}} - U_2) \cdot D}{L \cdot f_{\mathrm{s}}}.$$

Solving this equation with respect to L yields

$$L = \frac{(U_1 - U_\mathrm{T} - U_2) \cdot D}{\Delta i_\mathrm{L} \cdot f_\mathrm{s}} = \frac{(60\ \mathrm{V} - 2\ \mathrm{V} - 5.1\ \mathrm{V}) \cdot 0.1}{0.98\ \mathrm{A} \cdot 100\ \mathrm{kHz}} = 54\ \mathrm{\mu H}.$$

1.4 In the event of a malfunction, the speed and position sensors fail. As a result, the current $I_{2,\mathrm{fault}}$ drops to a value of 0.25 A. Which conduction mode will the converter enter, and what are the resulting consequences? Calculate the output voltage for this fault condition. The voltage losses off the diode and transistor shall not be considered [2 Points]

Answer:

The output current is less than the minimal current in BCM. This leads to DCM, which causes an overvoltage. The output voltage is to be calculated by the equation for DCM:

$$\begin{aligned}
U_2 &= \frac{D^2 \cdot T_\mathrm{s} \cdot U_1^2}{D^2 \cdot T_\mathrm{s} \cdot U_1^2 + 2 \cdot L \cdot \bar{i}_{2,\mathrm{fault}}} \\
&= \frac{D^2 \cdot U_1^2}{D^2 \cdot U_1^2 + 2 \cdot L \cdot \bar{i}_{2,\mathrm{fault}} \cdot f_\mathrm{s}} \\
&= \frac{0.085^2 \cdot 60\ \mathrm{V}^2}{0.085^2 \cdot 60\ \mathrm{V}^2 + 2 \cdot 54\ \mathrm{\mu H} \cdot 0.25\ \mathrm{A} \cdot 100\ \mathrm{kHz}} \\
&= 8.3\ \mathrm{V}.
\end{aligned}$$

Task 2: Buck-boost converter as smart voltage stabilizer for bicycle dynamo [10 Points]

A buck-boost converter is to be designed for voltage stabilization in a bicycle dynamo. The dynamo generator supplies a variable voltage. A control circuit adjusts the converter's duty cycle so that the buck-boost converter provides a stable output voltage.

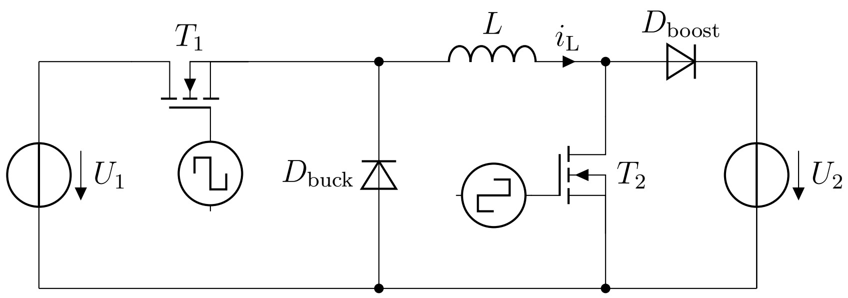


Fig. 2: Buck-boost converter circuit.

General parameters:		**MOSFET:**	
Input voltage:	$U_1 = 3\ \text{V} \dots 10\ \text{V}$	Transistor drain source voltage:	$u_{\text{ds,on}} = 0.5\ \text{V}$
Output voltage:	$U_2 = 5\ \text{V}$		
Output current range:	$I_2 = 50\ \text{mA} \dots 1\ \text{A}$	**Diode:**	
Switching frequency:	$f_{\text{s}} = 100\ \text{kHz}$	Diode forward voltage:	$u_{\text{fw}} = 0.8\ \text{V}$

The diode forward voltage and transistor voltage loss must be taken into account.
The drain-source voltage is valid for both transistors in conduct case..
The output voltage can be considered as constant except of subtask 2.4.

Tab. 2: Parameters of the circuit.

2.1 What are the minimum and maximum duty cycles that the control circuit has to request in case of $D = D_1 = D_2$? [2 Points]

Answer:

The synchronized duty cycle for the buck-boost converter is calculated using the inductor current balance equation

$$\Delta i_{\text{L,T}_{\text{on}}} \cdot T_{\text{on}} = \Delta i_{\text{L,T}_{\text{off}}} \cdot T_{\text{off}}.$$

If the transistors conduct $\Delta i_{\text{L,T}_{\text{on}}}$ results in:

$$\Delta i_{\text{L,T}_{\text{on}}} = \frac{(U_1 - 2u_{\text{ds,on}}) \cdot T_{\text{on}}}{L}.$$

If the transistors are blocking $\Delta i_{\text{L,T}_{\text{off}}}$ is calculated by:

$$\Delta i_{\text{L,T}_{\text{off}}} = \frac{(U_2 + 2u_{\text{fw}}) \cdot T_{\text{off}}}{L}.$$

By substituting the currents within the inductor current balance equation, we obtain

$$\frac{(U_1 - 2u_{\mathrm{ds,on}}) \cdot T_{\mathrm{on}}}{L} = \frac{(U_2 + 2u_{\mathrm{fw}}) \cdot T_{\mathrm{off}}}{L}.$$

Replacing T_{on} and T_{off} by the switching period yields to

$$\frac{(U_1 - 2u_{\mathrm{ds,on}}) \cdot T_{\mathrm{s}} \cdot D}{L} = \frac{(U_2 + 2u_{\mathrm{fw}}) \cdot (1-D) \cdot T_{\mathrm{s}}}{L}.$$

After simplifying by canceling T_{s} and L, we obtain

$$(U_1 - 2u_{\mathrm{ds,on}}) \cdot D = (U_2 + 2u_{\mathrm{fw}}) \cdot (1-D).$$

Solving this equation with respect to D yields

$$D = \frac{U_2 + 2u_{\mathrm{fw}}}{U_1 - 2u_{\mathrm{ds,on}} + U_2 + 2u_{\mathrm{fw}}}.$$

Entering the minimum and maximum input voltage leads yields

$$D_{\mathrm{max}} = \frac{5\ \mathrm{V} + 2 \cdot 0.8\ \mathrm{V}}{3\ \mathrm{V} - 2 \cdot 0.5\ \mathrm{V} + 5\ \mathrm{V} + 2 \cdot 0.8\ \mathrm{V}} = 0.77$$
$$D_{\mathrm{min}} = \frac{5\ \mathrm{V} + 2 \cdot 0.8\ \mathrm{V}}{10\ \mathrm{V} - 2 \cdot 0.5\ \mathrm{V} + 5\ \mathrm{V} + 2 \cdot 0.8\ \mathrm{V}} = 0.42.$$

2.2 Calculate the efficiency of the converter at the operation points $U_1 = 3$ V, $U_1 = 7.5$ V, and $U_1 = 10$ V at maximum output power. Consider only the losses due to the constant voltage drops of the semiconductors. [3 Points]

Answer:

The power loss are be separated in 2 parts: Power loss of the transistors while T_{on}-phase and power loss of the diodes while T_{off}-phase. The average current of the inductance is the same for both parts and yields

$$\bar{i}_{\mathrm{L}} = \frac{I_2}{1-D}.$$

The duty cycle of operation point $U_1 = 7.5$ V results in

$$D = \frac{U_2 + 2u_{\mathrm{fw}}}{U_1 - 2u_{\mathrm{ds,on}} + U_2 + 2u_{\mathrm{fw}}} = \frac{5\ \mathrm{V} + 2 \cdot 0.8\ \mathrm{V}}{7.5\ \mathrm{V} - 2 \cdot 0.5\ \mathrm{V} + 0.8\ \mathrm{V} + 5\ \mathrm{V} + 2 \cdot 0.8\ \mathrm{V}} = 0.5.$$

The power loss is calculated by

$$P_{\mathrm{loss}} = P_{\mathrm{loss,on}} + P_{\mathrm{loss,off}} = \bar{i}_{\mathrm{L}}(2u_{\mathrm{ds,on}} \cdot D + 2u_{\mathrm{fw}} \cdot (1-D)).$$

For the operation points we obtain

$$P_{\mathrm{loss,U_1=3\ V}} = \frac{1\ \mathrm{A}}{1-0.77}(2\cdot 0.5\ \mathrm{V}\cdot 0.77 + 2\cdot 0.5\ \mathrm{V}\cdot(1-0.77)) = 4.9\ \mathrm{W},$$
$$P_{\mathrm{loss,U_1=7.5\ V}} = \frac{1\ \mathrm{A}}{1-0.5}(2\cdot 0.5\ \mathrm{V}\cdot 0.5 + 2\cdot 0.5\ \mathrm{V}\cdot(1-0.5)) = 2.6\ \mathrm{W},$$
$$P_{\mathrm{loss,U_1=10\ V}} = \frac{1\ \mathrm{A}}{1-0.42}(2\cdot 0.5\ \mathrm{V}\cdot 0.42 + 2\cdot 0.5\ \mathrm{V}\cdot(1-0.42)) = 2.3\ \mathrm{W}.$$

The effciency is calculated by

$$\eta = \frac{P_2}{P_2 + P_{\mathrm{loss}}} = \frac{U_2 I_2}{U_2 I_2 + P_{\mathrm{loss}}}.$$

For the operation points we obtain

$$\eta_{\mathrm{U_1=3\ V}} = \frac{5\ \mathrm{V}\cdot 1\ \mathrm{A}}{5\ \mathrm{V}\cdot 1\ \mathrm{A} + 4.9\ \mathrm{W}} = 0.51,$$
$$\eta_{\mathrm{U_1=7.5\ V}} = \frac{5\ \mathrm{V}\cdot 1\ \mathrm{A}}{5\ \mathrm{V}\cdot 1\ \mathrm{A} + 2.6\ \mathrm{W}} = 0.66,$$
$$\eta_{\mathrm{U_1=10\ V}} = \frac{5\ \mathrm{V}\cdot 1\ \mathrm{A}}{5\ \mathrm{V}\cdot 1\ \mathrm{A} + 2.3\ \mathrm{W}} = 0.68.$$

2.3 To avoid operation in discontinuous conduction mode (DCM) within the defined operating range, the minimum inductance L must be calculated. Evaluate the general equation for boundary conduction mode (BCM) to indicate, at which operation point the discontinuous conduction mode starts? $D = D_1 = D_2$ still applies. [2 Points]

Answer:

The ripple current is calculated by

$$\Delta i_{\mathrm{L}} = \frac{U_{\mathrm{L,off}}\cdot T_{\mathrm{off}}}{L} = \frac{(U_2 + 2u_{\mathrm{fw}})\cdot(1-D)}{L\cdot f_{\mathrm{s}}}.$$

Remark: The duty cycle depends on input voltage U_1. Therefore the fix output voltage U_2 is utilized. At boundary conduction mode (BCM) the ripple current yields

$$\Delta i_{\mathrm{L}} = \frac{2I_2}{1-D}.$$

This leads to

$$\frac{(U_2 + 2u_{\mathrm{fw}})\cdot(1-D)}{L\cdot f_{\mathrm{s}}} = \frac{2I_2}{1-D}.$$

Solving the equation with respect to L leads to

$$L = \frac{(U_2 + 2u_{\mathrm{fw}}) \cdot (1 - D)^2}{2I_2 \cdot f_{\mathrm{s}}}.$$

The term $(1-D)^2$ express, that at minimum duty cycle the highest inductance is needed, to prevent discontinuous conduction mode. Therefore D_{min} is used delivering

$$L = \frac{(5\ \mathrm{V} + 2 \cdot 0.8\ \mathrm{V}) \cdot (1 - 0.42)^2}{2 \cdot 50\ \mathrm{mA} \cdot 100\ \mathrm{kHz}} = 219\ \mathrm{\mu H}.$$

2.4 Now the control circuit regulates the transistors independent. It means, for low input voltage the boost mode is used and for high input voltage the buck mode is uses. How are the duty cycles D_1 of transistor T_1 and D_2 of transistor T_2 for the operating points? [3 Points]

Answer:

In boost mode the duty cycle $D_1 = 1$ so that T_1 always conducts. The boost mode is active if $U_1 - u_{\mathrm{ds,on}}$ is less equal $U_2 + 2u_{\mathrm{fw}}$. The break-even point is calculated by

$$U_1 = U_2 + u_{\mathrm{fw}} + u_{\mathrm{ds,on}} = 5\ \mathrm{V} + 0.8\ \mathrm{V} + 0.5\ \mathrm{V} = 6.3\ \mathrm{V}.$$

The duty cycle for the boost mode is calculated using the inductor current balance equation

$$\Delta i_{\mathrm{L,T_{on}}} \cdot T_{\mathrm{on}} = \Delta i_{\mathrm{L,T_{off}}} \cdot T_{\mathrm{off}}.$$

If the transistors conduct $\Delta i_{\mathrm{L,T_{on}}}$ results in:

$$\Delta i_{\mathrm{L,T_{on}}} = \frac{(U_1 - 2u_{\mathrm{ds,on}}) \cdot T_{\mathrm{on}}}{L}.$$

If the transistor T_2 is blocking $\Delta i_{\mathrm{L,T_{off}}}$ is calculated by:

$$\Delta i_{\mathrm{L,T_{off}}} = \frac{(U_2 + u_{\mathrm{fw}} + u_{\mathrm{ds,on}} - U_1) \cdot T_{\mathrm{off}}}{L}.$$

By substituting the currents within the inductor current balance equation we obtain

$$\frac{(U_1 - 2u_{\mathrm{ds,on}}) \cdot T_{\mathrm{on}}}{L} = \frac{(U_2 + u_{\mathrm{fw}} + u_{\mathrm{ds,on}} - U_1) \cdot T_{\mathrm{off}}}{L}.$$

Replacing T_{on} and T_{off} by the switching period yields to

$$\frac{(U_1 - 2u_{\mathrm{ds,on}}) \cdot T_{\mathrm{s}} \cdot D_2}{L} = \frac{(U_2 + u_{\mathrm{fw}} + u_{\mathrm{ds,on}} - U_1) \cdot (1 - D_2) \cdot T_{\mathrm{s}}}{L}.$$

After simplifying by canceling T_s and L we obtain

$$(U_1 - 2u_\mathrm{ds,on}) \cdot D_2 = (U_2 + u_\mathrm{fw} + u_\mathrm{ds,on} - U_1) \cdot (1 - D_2).$$

Solving this equation with respect to D_2 yields

$$D_2 = \frac{U_2 + u_\mathrm{fw} + u_\mathrm{ds,on} - U_1}{U_2 + u_\mathrm{fw} - u_\mathrm{ds,on}}.$$

For the operation point $U_1 = 3$ V we obtain

$$D_{2,\mathrm{U_1=3\ V}} = \frac{5\ \mathrm{V} + 0.8\ \mathrm{V} + 0.5\ \mathrm{V} - 3\ \mathrm{V}}{5\ \mathrm{V} + 0.8\ \mathrm{V} - 0.5\ \mathrm{V}} = 0.62.$$

In buck mode the duty cycle $D_2 = 0$ so that T_2 always blocks. The duty cycle for the buck mode is calculated using the inductor current balance equation

$$\Delta i_{\mathrm{L,T_{on}}} \cdot T_\mathrm{on} = \Delta i_{\mathrm{L,T_{off}}} \cdot T_\mathrm{off}.$$

If the transistor T_1 conducts $\Delta i_{\mathrm{L,T_{on}}}$ results in:

$$\Delta i_{\mathrm{L,T_{on}}} = \frac{(U_1 - u_\mathrm{ds,on} - u_\mathrm{fw} - U_2) \cdot T_\mathrm{on}}{L}.$$

If the transistor T_1 is blocking $\Delta i_{\mathrm{L,T_{off}}}$ is calculated by:

$$\Delta i_{\mathrm{L,T_{off}}} = \frac{(U_2 + 2u_\mathrm{fw}) \cdot T_\mathrm{off}}{L}.$$

By substituting the currents within the inductor current balance equation, we obtain

$$\frac{(U_1 - u_\mathrm{ds,on} - u_\mathrm{fw} - U_2) \cdot T_\mathrm{on}}{L} = \frac{(U_2 + 2u_\mathrm{fw}) \cdot T_\mathrm{off}}{L}.$$

Replacing T_on and T_off by the switching period yields to

$$\frac{(U_1 - u_\mathrm{ds,on} - u_\mathrm{fw} - U_2) \cdot T_\mathrm{s} \cdot D_1}{L} = \frac{(U_2 + 2u_\mathrm{fw}) \cdot (1 - D_1) \cdot T_\mathrm{s}}{L}.$$

After simplifying by canceling T_s and L, we obtain

$$(U_1 - u_\mathrm{ds,on} - u_\mathrm{fw} - U_2) \cdot D_1 = (U_2 + 2u_\mathrm{fw}) \cdot (1 - D_1).$$

Solving this equation with respect to D_1 yields

$$D_1 = \frac{U_2 + 2u_\mathrm{fw}}{U_1 - u_\mathrm{ds,on} + u_\mathrm{fw}}.$$

For the operation points $U_1 = 7.5$ V and $U_1 = 10$ V we obtain

$$D_{1,\mathrm{U_1=7.5\ V}} = \frac{5\ \mathrm{V} + 2 \cdot 0.8\ \mathrm{V}}{7.5\ \mathrm{V} - 0.5\ \mathrm{V} + 0.8\ \mathrm{V}} = 0.85,$$
$$D_{1,\mathrm{U_1=10\ V}} = \frac{5\ \mathrm{V} + 2 \cdot 0.8\ \mathrm{V}}{10\ \mathrm{V} - 0.5\ \mathrm{V} + 0.8\ \mathrm{V}} = 0.64.$$

Task 3: Thyristor-based AC/DC converter (M2C) [13 Points]

In an electroplating process, a single-phase two-pulse midpoint thyristor converter (M2C) with center-tapped transformer is used as a controllable DC source. After product quality issues, the engineering team must verify whether the converter is operated with suitable firing angles and acceptable grid impact.

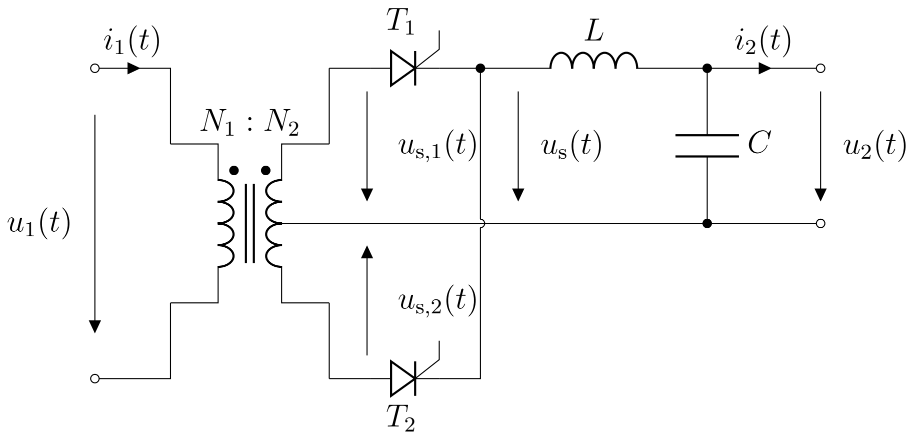


Fig. 3: M2C converter with an output filter assuming $u_2(t) = U_2 = \text{const.}$

Parameter	Symbol	Value
Primary grid voltage (RMS)	U_1	230 V
Grid frequency	f_1	50 Hz
Transformer turns ratio	N_2/N_1	1.0
Firing angle (normal operation)	α_0	70°
DCM conduction angle (low-load case)	β	140°
Average output current (CCM)	I_2	30 A
Required plating voltage setpoint	$\overline{u}_{2,\text{set}}$	75 V

Tab. 3: M2C operation parameters.

3.1 In continuous conduction mode (CCM), calculate the average output voltage $\overline{u}_{2,\text{CCM}}$ for the firing angle $\alpha_0 = 70°$. [2 Points]

Answer:
Calculate the peak voltage using:

$$\hat{u}_1 = \sqrt{2}U_1 = 325.27\ \text{V}, \qquad \hat{u}_\text{s} = \frac{1}{2}\hat{u}_1 = 162.63\ \text{V}.$$

Then the output voltage in CCM at α_0 is:

$$\overline{u}_{2,\text{CCM}} = \hat{u}_\text{s}\frac{2}{\pi}\cos\alpha_0 = 103.54\ \text{V}\cdot\cos(70°) = 35.41\ \text{V}.$$

3.2 To correctly set the firing angle in CCM, determine α_set for $\overline{u}_{2,\text{set}} = 75$ V. [1 Point]

Answer:
Firing angle for $\overline{u}_{2,\mathrm{set}}$ in CCM:

$$\overline{u}_{2,\mathrm{set}} = \hat{u}_\mathrm{s}\frac{2}{\pi}\cos\alpha_\mathrm{set} \Rightarrow \cos\alpha_\mathrm{set} = \frac{75\ \mathrm{V}}{103.54\ \mathrm{V}} = 0.7244, \quad \alpha_\mathrm{set} \approx 43.6°.$$

3.3 In open-loop operation with fixed firing angle α, explain why the converter can enter discontinuous conduction mode (DCM) at low load, why this complicates maintaining a constant plating voltage, and how this affects the final quality. [2 Points]

Answer:
At low load, the demanded output current decreases and can reach zero before the next thyristor pair is triggered. This interrupts conduction and the converter changes from CCM to DCM. In DCM, the average output voltage depends not only on α but also on the load-dependent conduction interval (β). So a fixed firing angle can no longer guarantee a constant plating voltage, causing unpredictable plating conditions and inconsistent product quality.

3.4 Assuming low-load operation, the converter enters DCM with $\beta = 140°$. Calculate $\overline{u}_{2,\mathrm{DCM}}$ for α_set from subtask 3.2, and compare it to the required setpoint $\overline{u}_{2,\mathrm{set}} = 75$ V. Briefly explain how to avoid load-dependent output voltage. [2 Points]
Hint: If you did not find α_set in subtask 3.2, use α_0 instead.

Answer:
Average output voltage in DCM, at α_set, β:

$$\overline{u}_{2,\mathrm{DCM}} = \hat{u}_\mathrm{s}\frac{2}{\pi}\sin\left(\frac{\beta}{2}\right)\sin\left(\alpha_\mathrm{set} + \frac{\beta}{2}\right) = 103.54\ \mathrm{V}\cdot\sin(70°)\cdot\sin(113.6°) = 89.06\ \mathrm{V}.$$

The DCM value exceeds the required setpoint of 75 V and is load-dependent. Either, choose higher inductance to avoid DCM at low load, or implement closed-loop control to adjust α and maintain the setpoint regardless of load variations.

3.5 At this new operating point ($\alpha = \alpha_\mathrm{set}$, $I_2 = 30$ A), calculate the fundamental current $I_1^{(1)}$ and power components P_1, $Q_1^{(1)}$, and $S_1^{(1)}$. [3 Points]
Hint: If you did not find α_set in subtask 3.2, use α_0 instead.

Answer:
Fundamental complex power at α_set:
Given that

$$\frac{N2}{N1} = 1.$$

Then

$$I_1^{(1)} = \frac{\sqrt{2}}{\pi}I_2 = 13.50\ \mathrm{A}.$$

$$S_1^{(1)} = I_2 \hat{u}_{s0} = 3106 \text{ VA}, \qquad \text{where} \quad \hat{u}_{s0} = \hat{u}_s \frac{2}{\pi}$$

$$P_1 = I_2 \hat{u}_{s0} \cos \alpha_{\text{set}} = 2250 \text{ W}, \qquad Q_1^{(1)} = I_2 \hat{u}_{s0} \sin \alpha_{\text{set}} = 2142 \text{ VA}.$$

3.6 Including harmonics, calculate total apparent power S_1 and total reactive power Q_1, and briefly assess whether the harmonic share is significant for grid compliance. [3 Points]

Answer:

Including harmonics we receive:

$$S_1 = \frac{\pi}{2\sqrt{2}} S_1^{(1)} = 3450 \text{ VA},$$

$$Q_1 = \sqrt{S_1^2 - P_1^2} = 2615 \text{ VA}.$$

Since the harmonic share is $S_1/S_1^{(1)} = \pi/(2\sqrt{2}) \approx 1.11$, the harmonics contribute about 11% to the total apparent power, which is significant and must be considered relevant for grid compliance.

Task 4: Transistor-based AC/DC converter (single-phase AFE) [11 Points]

An electric-drive test bench is connected to a single-phase grid via a full-bridge transistor AFE rectifier. The converter should operate with approximately unity power factor and a stable DC-link voltage. During testing, increased DC-link ripple is observed and the PWM strategy is questioned.

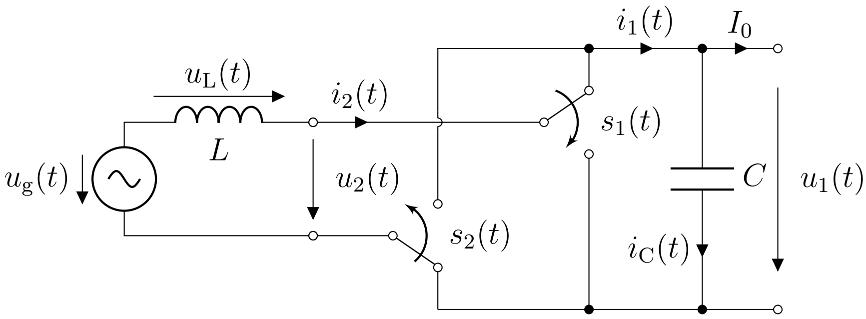


Fig. 4: Single-phase grid rectification. Also known as active front end (AFE) rectifier.

Parameter	Symbol	Value
Grid voltage (RMS)	U_g	230 V
Grid frequency	f	50 Hz
Grid-side inductance	L	2.5 mH
DC-link voltage	U_{dc}	450 V
Active power setpoint	P	3.0 kW
DC-link capacitor	C_{dc}	2.2 mF
Switching period	T_s	100 µs
PWM reference signal	$s^*(t)$	sinusoidal

Tab. 4: Nominal operating parameters of the single-phase AFE rectifier.

4.1 For approximately unity power factor operation, determine the required grid current RMS value and the corresponding grid current peak value. [2 Points]

Answer:

Grid current at unity power factor is:

$$P = U_g I_g \Rightarrow I_g = \frac{3000\ \mathrm{W}}{230\ \mathrm{V}} = 13.04\ \mathrm{A}.$$

$$\hat{i}_g = \sqrt{2} I_g = 18.44\ \mathrm{A}.$$

4.2 Calculate the required converter input-voltage amplitude $\hat{u}_2$ and verify whether the nominal DC-link voltage is feasible. [1 Point]

Answer:

Required converter input-voltage amplitude yields:

$$\hat{u}_2 = \sqrt{\hat{u}_g^2 + (\omega L \hat{i}_g)^2} = \sqrt{(325.27\ \mathrm{V})^2 + \left(314.16\ \tfrac{1}{\mathrm{s}} \cdot 2.5\ \mathrm{mH} \cdot 18.44\ \mathrm{A}\right)^2} = 325.59\ \mathrm{V}.$$

With $U_{dc} = 450\ \mathrm{V} > \hat{u}_2$, the boost rectifier condition is fulfilled.

4.3 Determine the DC-link voltage oscillation amplitude $\hat{u}_C$. [4 Points]

Answer:

Calculating the DC-link ripple requires the apparent power at the converter input:

$$Q_2 = \omega L I_g^2 = 314.16\ \tfrac{1}{\mathrm{s}} \cdot 2.5\ \mathrm{mH} \cdot (13.04\ \mathrm{A})^2 = 133.7\ \mathrm{VA}.$$

$$S_2 = \sqrt{P^2 + Q_2^2} = \sqrt{(3000\ \mathrm{W})^2 + (133.7\ \mathrm{VA})^2} = 3003\ \mathrm{VA}.$$

From lecture Eq. (6.23), the DC-link current ripple amplitude is approximately

$$\hat{i}_C \approx \frac{S_2}{U_{dc}} = \frac{3003}{450} = 6.67\ \mathrm{A}.$$

Hence, the DC-link voltage ripple amplitude results in

$$\hat{u}_C \approx \frac{\hat{i}_C}{2\omega C_{dc}} = \frac{6.67\ \mathrm{A}}{2 \cdot 314.16\ \tfrac{1}{\mathrm{s}} \cdot 2.2\ \mathrm{mF}} = 4.82\ \mathrm{V}.$$

Alternatively, The average DC-link current follows from the active power balance:

$$I_0 = \frac{P}{U_{dc}} = \frac{3000\ \mathrm{W}}{450\ \mathrm{V}} = 6.67\ \mathrm{A}.$$

The DC-link voltage ripple amplitude is

$$\hat{u}_C = \hat{u}_1 \approx \frac{\hat{i}_C}{2\omega C_{dc}} = \frac{I_0}{2\omega C_{dc}} \sqrt{1 + \left(\frac{\omega L U_{dc}}{U_g^2}\right)^2}.$$

Substituting the values yields

$$\hat{u}_C = \frac{6.67\ \mathrm{A}}{2 \cdot 314.16\ \tfrac{1}{\mathrm{s}} \cdot 2.2\ \mathrm{mF}} \sqrt{1 + \left(\frac{314.16\ \tfrac{1}{\mathrm{s}} \cdot 2.5\ \mathrm{mH} \cdot 450\ \mathrm{V}}{230\ \mathrm{V}^2}\right)^2} = 4.82\ \mathrm{V}.$$

4.4 The engineering team suspects that the choice of PWM strategy contributes to the observed DC-link ripple. Using a sinusoidal reference $s^*(t) = \hat{s}\sin(\omega t)$ and a triangular carrier $c(t) \in [-1, 1]$, sketch the switching states of both complementary PWM and interleaved PWM over one fundamental electrical period ($\omega t \in [0, 2\pi]$) in the provided templates. Finally, explain which strategy produces a lower AC-side current ripple in L and why this reduces stress on the DC-link capacitor C_{dc}. [4 Points]

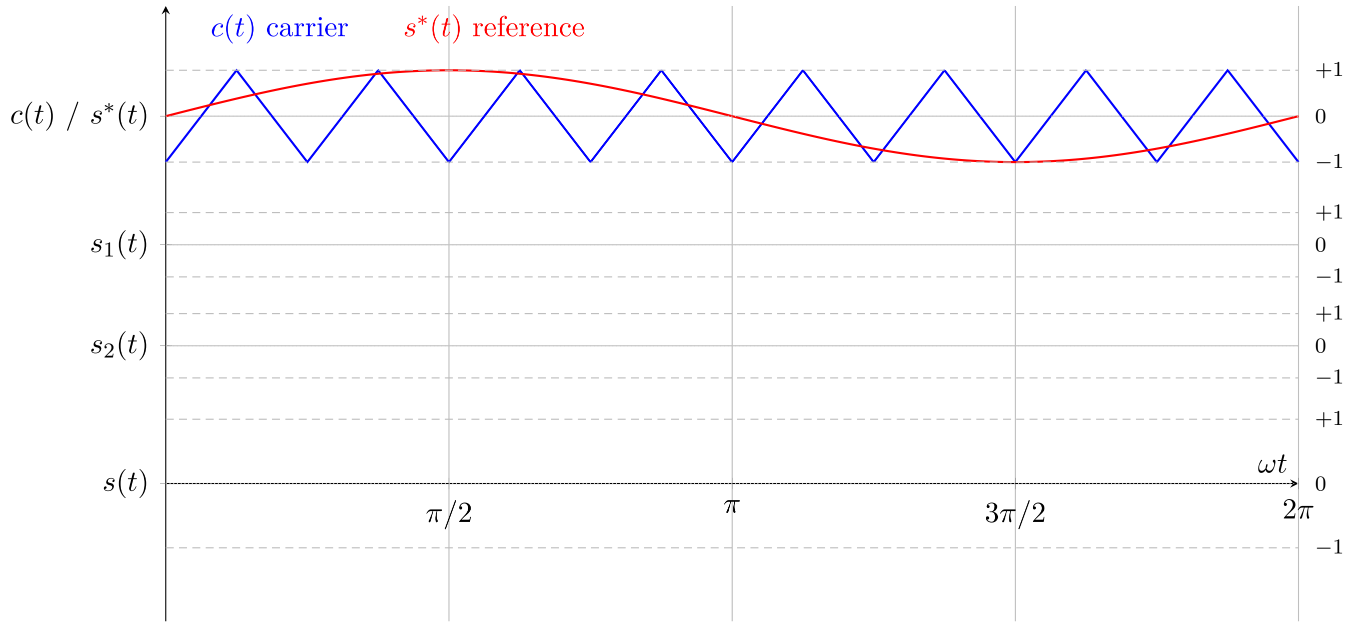


Fig. 5: Template: complementary PWM with sinusoidal reference $s^*(t)$ over one electrical period ($\omega t \in [0, 2\pi]$).

Answer:

Given: The modulation reference is sinusoidal, $s^*(t) = \hat{s}\sin(\omega t)$. The sketches are shown over one fundamental electrical period ($\omega t \in [0, 2\pi]$).

1) Complementary PWM

$$s_1(t) = \begin{cases} +1, & s^*(t) > c(t) \\ -1, & s^*(t) \le c(t) \end{cases}, \qquad s_2(t) = -s_1(t).$$

The equivalent converter state is

$$s_{\mathrm{cs}}(t) = \frac{s_1(t) - s_2(t)}{2} = s_1(t) \in \{+1, -1\}.$$

2) Interleaved PWM

$$s_1(t) = \begin{cases} +1, & s^*(t) > c(t) \\ -1, & s^*(t) \le c(t) \end{cases}, \qquad s_2(t) = \begin{cases} +1, & -s^*(t) > c(t) \\ -1, & -s^*(t) \le c(t) \end{cases}.$$

The equivalent three-level state is

$$s_{\mathrm{is}}(t) = \frac{s_1(t) - s_2(t)}{2} \in \{+1, 0, -1\}.$$

A correct sketch over one electrical period shows transition instants at the intersections of $c(t)$ with $s^*(t)$ and $-s^*(t)$.

What must be visible in the plots:

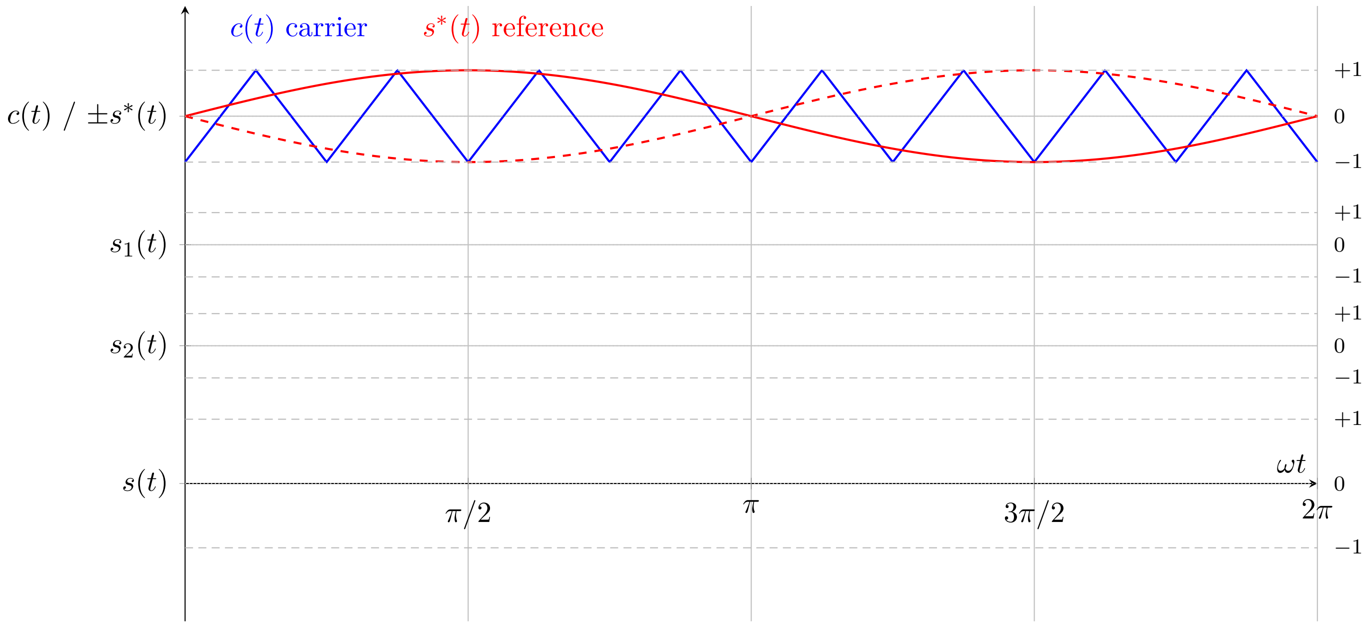
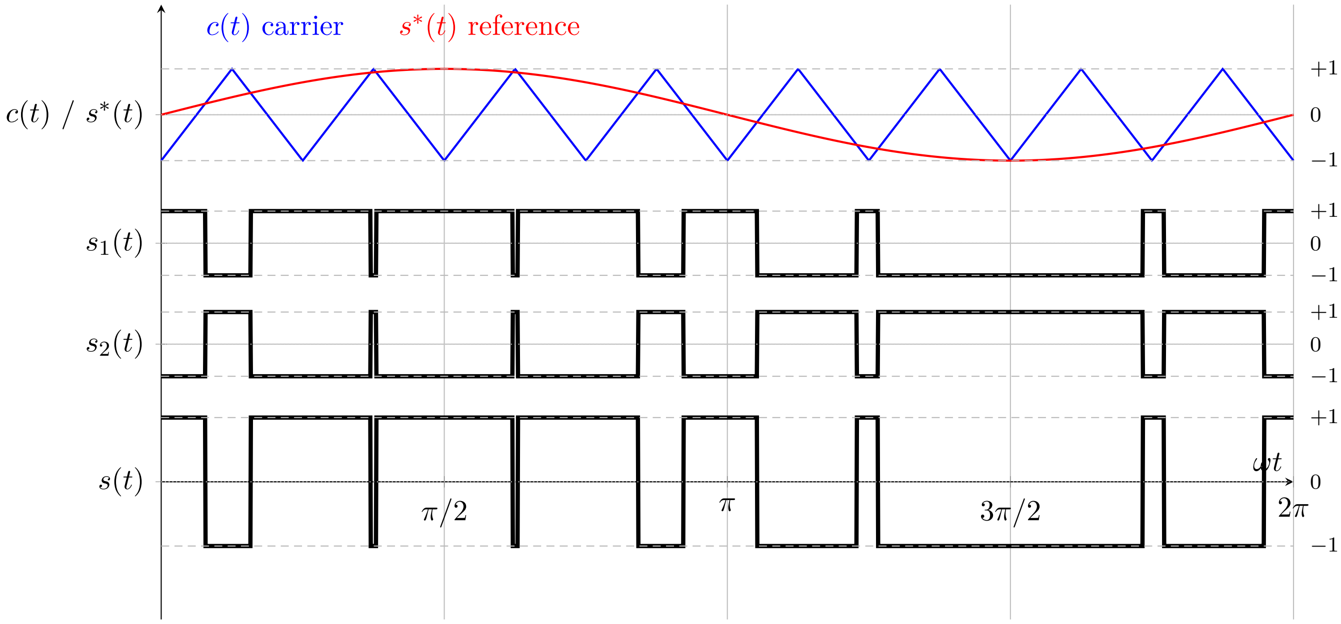


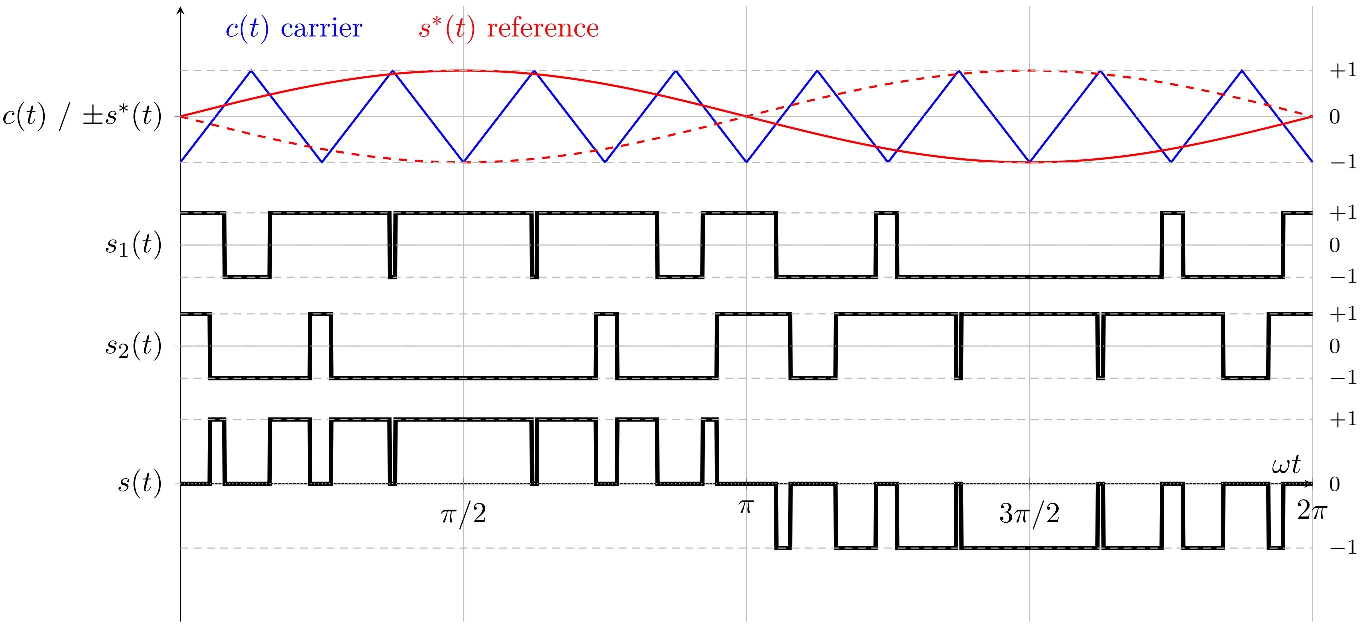
Fig. 6: Template: interleaved PWM with one carrier and references $s^*(t)$ and $-s^*(t)$ over one electrical period ($\omega t \in [0, 2\pi]$).

- Complementary PWM: one carrier $c(t)$, one reference $s^*(t)$, states s_1, s_2, and resulting $s \in \{+1, -1\}$.
- Interleaved PWM: one carrier $c(t)$, both references $s^*(t)$ and $-s^*(t)$, states s_1, s_2, and resulting $s \in \{+1, 0, -1\}$.

Comparison and impact on DC-link ripple:
Complementary PWM produces a two-level converter output state (± 1), while interleaved PWM produces a three-level output state $(+1, 0, -1)$. The additional zero level in interleaved PWM reduces the effective voltage steps across L and therefore reduces the AC-side current ripple. Since the high-frequency capacitor current is caused by the switching ripple power of the converter, the smaller inductor current ripple of interleaved PWM reduces the current stress of C_{dc} and therefore lowers the DC-link voltage ripple $\Delta U_{dc,pp}$ observed in the previous subtask. Interleaved PWM is therefore the preferable strategy.



Solution Fig. 1: Solution plot: complementary PWM and switching state over one electrical period ($\omega t \in [0, 2\pi]$).



Solution Fig. 2: Solution plot: interleaved PWM and equivalent switching state over one electrical period ($\omega t \in [0, 2\pi]$).