Exam

Power Electronics

Winter 2025/26

First name: Last name:

Matriculation number: Study program:

Instructions:

- You can only take part in the exam, if you are registered in the campus management system.
- Prepare your student ID and a photo ID card on your desk.
- Label each exam sheet with your name. Start a new exam sheet for each task.
- Answers must be given with a complete, comprehensible solution. Answers without any context will not be considered. Answers are accepted in German and English.
- Permitted tools are (exclusively): black / blue pens (indelible ink), triangle, a non-programmable calculator without graphic display and two DIN A4 cheat sheets.
- The exam time is 120 minutes.

Evaluation:

Task	1	2	3	4	$\sum$
Maximum score	8	10	13	11	42
Achieved score					

Task 1: Step-down converter **[8 Points]**

A drive system is powered by DC-voltage. The speed, position, and current sensors in the drive system require stable lower voltage. To transform the voltage down efficiently, a buck converter is used.

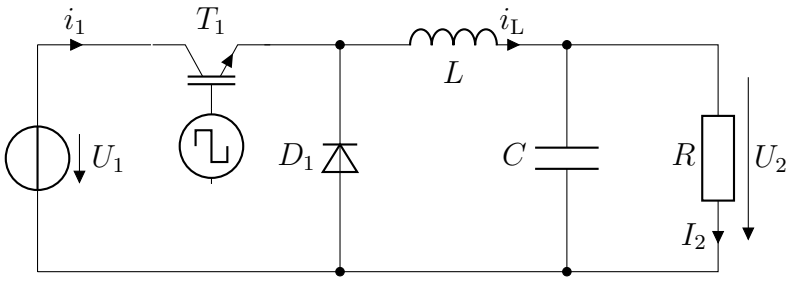

Fig. 1: Circuit with one transistor, filter and one load resistor.

General parameters:		**IGBT:**	
Input voltage:	$U_1 = 60$ V	Collector-emitter voltage:	$u_{\text{on,CE}} = 2$ V
Output voltage:	$U_2 = 5.1$ V		
Output power:	$2.5\text{ W} \leq p \leq 15\text{ W}$	**Diode:**	
Switching frequency:	$f_\text{s} = 100$ kHz	Forward voltage:	$u_\text{fw} = 0.8$ V

Tab. 1: Parameters of the step-down converter.

1.1 What duty cycle must be set for the given input-to-output voltage ratio, assuming ideal components? [1 Point]

1.2 What duty cycle is required when the voltage drops across the transistor and the diode are taken into account? [3 Points]

1.3 The sensors have different power consumption depending on the operating point, i.e., $P_2 \in [2.5\text{ W}, 15\text{ W}]$ is given. Which load operating point is the relevant one to design the inductance value L such that discontinuous conduction mode (DCM) is always avoided? Calculate the minimal required inductances L for this case. [2 Points]

1.4 In the event of a malfunction, the speed and position sensors fail. As a result, the current $I_{2,\text{fault}}$ drops to a value of 0.25 A. Which conduction mode will the converter enter, and what are the resulting consequences? Calculate the output voltage for this fault condition. The voltage losses off the diode and transistor shall not be considered [2 Points]

Task 2: Buck-boost converter as smart voltage stabilizer for bicycle dynamo [10 Points]

A buck-boost converter is to be designed for voltage stabilization in a bicycle dynamo. The dynamo generator supplies a variable voltage. A control circuit adjusts the converter's duty cycle so that the buck-boost converter provides a stable output voltage.

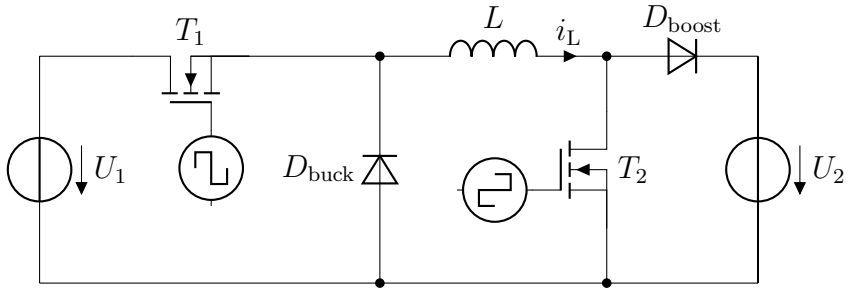

Fig. 2: Buck-boost converter circuit.

General parameters:		**MOSFET:**	
Input voltage:	$U_1 = 3\ \mathrm{V} \ldots 10\ \mathrm{V}$	Transistor drain source voltage:	$u_\mathrm{ds,on} = 0.5\ \mathrm{V}$
Output voltage:	$U_2 = 5\ \mathrm{V}$		
Output current range:	$I_2 = 50\ \mathrm{mA} \ldots 1\ \mathrm{A}$	**Diode:**	
Switching frequency:	$f_\mathrm{s} = 100\ \mathrm{kHz}$	Diode forward voltage:	$u_\mathrm{fw} = 0.8\ \mathrm{V}$

The diode forward voltage and transistor voltage loss must be taken into account.
The drain-source voltage is valid for both transistors in conduct case..
The output voltage can be considered as constant except of subtask 2.4.

Tab. 2: Parameters of the circuit.

2.1 What are the minimum and maximum duty cycles that the control circuit has to request in case of $D = D_1 = D_2$? [2 Points]

2.2 Calculate the efficiency of the converter at the operation points $U_1 = 3$ V, $U_1 = 7.5$ V, and $U_1 = 10$ V at maximum output power. Consider only the losses due to the constant voltage drops of the semiconductors. [3 Points]

2.3 To avoid operation in discontinuous conduction mode (DCM) within the defined operating range, the minimum inductance L must be calculated. Evaluate the general equation for boundary conduction mode (BCM) to indicate, at which operation point the discontinuous conduction mode starts? $D = D_1 = D_2$ still applies. [2 Points]

2.4 Now the control circuit regulates the transistors independent. It means, for low input voltage the boost mode is used and for high input voltage the buck mode is uses. How are the duty cycles D_1 of transistor T_1 and D_2 of transistor T_2 for the operating points? [3 Points]

Task 3: Thyristor-based AC/DC converter (M2C) [13 Points]

In an electroplating process, a single-phase two-pulse midpoint thyristor converter (M2C) with center-tapped transformer is used as a controllable DC source. After product quality issues, the engineering team must verify whether the converter is operated with suitable firing angles and acceptable grid impact.

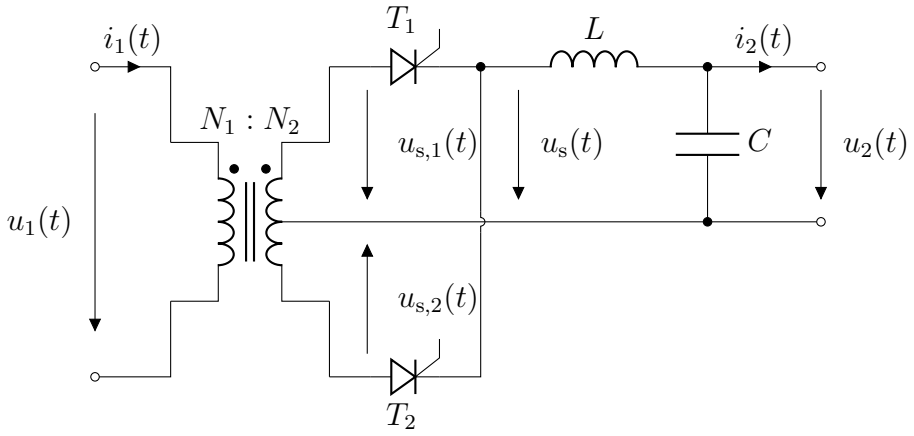

Fig. 3: M2C converter with an output filter assuming $u_2(t) = U_2 = \text{const.}$

Parameter	Symbol	Value
Primary grid voltage (RMS)	U_1	230 V
Grid frequency	f_1	50 Hz
Transformer turns ratio	N_2/N_1	1.0
Firing angle (normal operation)	α_0	70°
DCM conduction angle (low-load case)	β	140°
Average output current (CCM)	I_2	30 A
Required plating voltage setpoint	$\overline{u}_{2,\text{set}}$	75 V

Tab. 3: M2C operation parameters.

3.1 In continuous conduction mode (CCM), calculate the average output voltage $\overline{u}_{2,\text{CCM}}$ for the firing angle $\alpha_0 = 70°$. [2 Points]

3.2 To correctly set the firing angle in CCM, determine α_{set} for $\overline{u}_{2,\text{set}} = 75$ V. [1 Point]

3.3 In open-loop operation with fixed firing angle α, explain why the converter can enter discontinuous conduction mode (DCM) at low load, why this complicates maintaining a constant plating voltage, and how this affects the final quality. [2 Points]

3.4 Assuming low-load operation, the converter enters DCM with $\beta = 140°$. Calculate $\overline{u}_{2,\text{DCM}}$ for α_{set} from subtask 3.2, and compare it to the required setpoint $\overline{u}_{2,\text{set}} = 75$ V. Briefly explain how to avoid load-dependent output voltage. [2 Points]
Hint: If you did not find α_{set} in subtask 3.2, use α_0 instead.

3.5 At this new operating point ($\alpha = \alpha_{\text{set}}$, $I_2 = 30$ A), calculate the fundamental current $I_1^{(1)}$ and power components P_1, $Q_1^{(1)}$, and $S_1^{(1)}$. [3 Points]
Hint: If you did not find α_{set} in subtask 3.2, use α_0 instead.

3.6 Including harmonics, calculate total apparent power S_1 and total reactive power Q_1, and briefly assess whether the harmonic share is significant for grid compliance. [3 Points]

Task 4: Transistor-based AC/DC converter (single-phase AFE) [11 Points]

An electric-drive test bench is connected to a single-phase grid via a full-bridge transistor AFE rectifier. The converter should operate with approximately unity power factor and a stable DC-link voltage. During testing, increased DC-link ripple is observed and the PWM strategy is questioned.

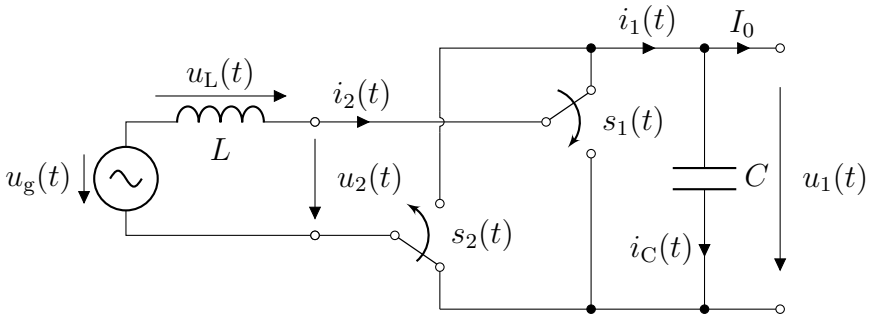

Fig. 4: Single-phase grid rectification. Also known as active front end (AFE) rectifier.

Parameter	Symbol	Value
Grid voltage (RMS)	U_g	230 V
Grid frequency	f	50 Hz
Grid-side inductance	L	2.5 mH
DC-link voltage	U_dc	450 V
Active power setpoint	P	3.0 kW
DC-link capacitor	C_dc	2.2 mF
Switching period	T_s	100 µs
PWM reference signal	$s^*(t)$	sinusoidal

Tab. 4: Nominal operating parameters of the single-phase AFE rectifier.

4.1 For approximately unity power factor operation, determine the required grid current RMS value and the corresponding grid current peak value. [2 Points]

4.2 Calculate the required converter input-voltage amplitude $\hat{u}_2$ and verify whether the nominal DC-link voltage is feasible. [1 Point]

4.3 Determine the DC-link voltage oscillation amplitude $\hat{u}_\mathrm{C}$. [4 Points]

4.4 The engineering team suspects that the choice of PWM strategy contributes to the observed DC-link ripple. Using a sinusoidal reference $s^*(t) = \hat{s}\sin(\omega t)$ and a triangular carrier $c(t) \in [-1, 1]$, sketch the switching states of both complementary PWM and interleaved PWM over one fundamental electrical period ($\omega t \in [0, 2\pi]$) in the provided templates. Finally, explain which strategy produces a lower AC-side current ripple in L and why this reduces stress on the DC-link capacitor C_dc. [4 Points]

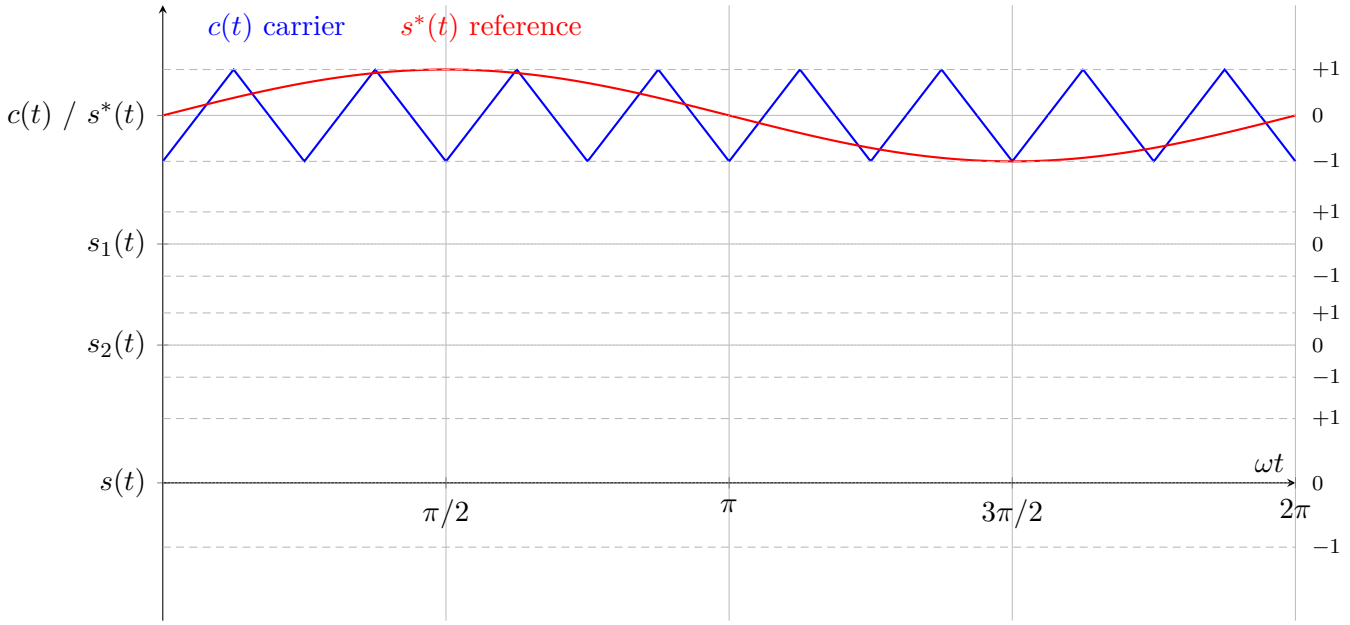

Fig. 5: Template: complementary PWM with sinusoidal reference $s^*(t)$ over one electrical period ($\omega t \in [0, 2\pi]$).

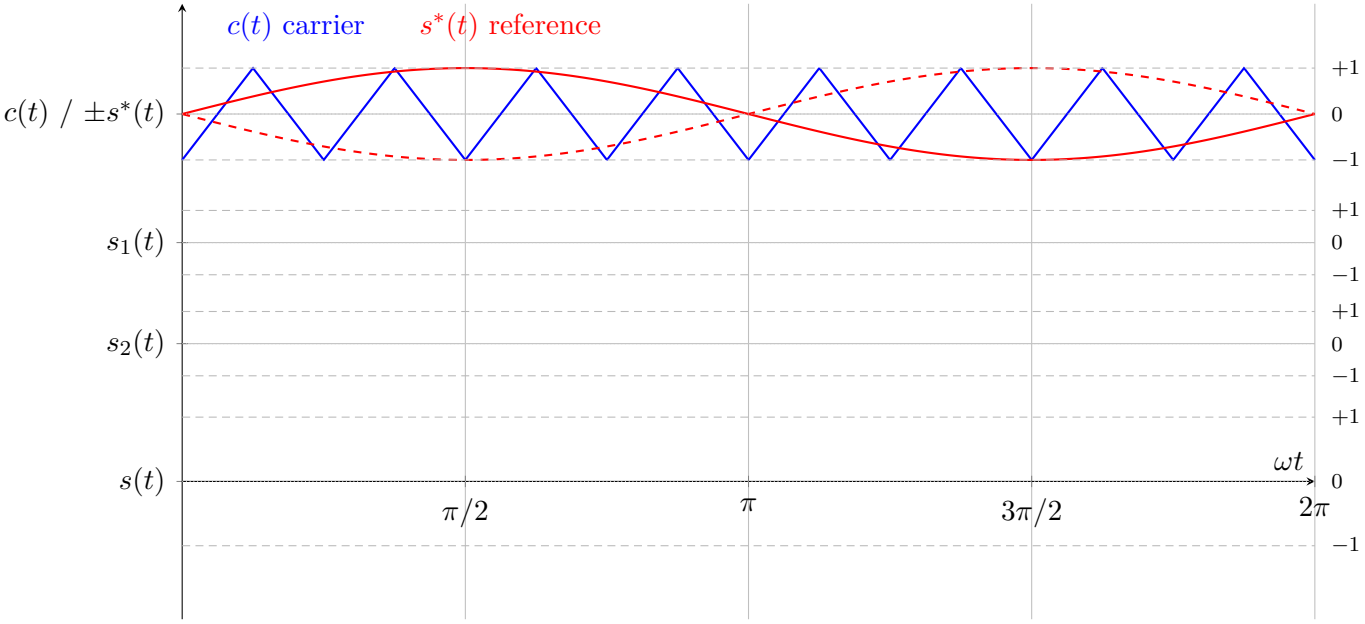

Fig. 6: Template: interleaved PWM with one carrier and references $s^*(t)$ and $-s^*(t)$ over one electrical period ($\omega t \in [0, 2\pi]$).